L Number	Hits	Search Text	DB	Time stamp
1	37	438/257,366,367,368,369,303.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:10
2	37	438/257,366,367,368,369,303.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:10
3	1	438/257,366,367,368,369.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and gate and (gate adj dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:14
4	0	438/257.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)and (gate adj stack) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:18
5	0	438/257.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)and (gate adj stack) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:19
6	0	438/257.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (spacer$2) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)and (gate adj stack) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:19
-	1	6753242.pn. and (electrode adj region)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:23
-	50	gate adj electrode and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (nitride adj spacers) and (channel adj region)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/08/31 13:42
-	36	gate adj electrode and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (nitride adj spacers) and (channel adj region) and @ad<20020319	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/08/31 14:17
-	36	gate adj electrode and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (nitride adj spacers) and (channel adj region) and @ad<20020319	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/08/31 14:41
-	1	20020028541.pn. and (nitride adj layer) and (oxide adj layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/08/31 14:36
-	1	20020028541.pn. and (nitride adj spacer) and (oxide adj spacer)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/08/31 14:36

-	13	gate adj electrode and (semiconductor adj substrate) and dielectric and source and drain and ((oxide adj spacers) same (nitride adj spacers)) and (channel adj region) and @ad<20020319	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 10:36
-	1	(gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)and (gate adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 10:39
-	0	(gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)and (gate adj stack) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:17
-	1	(gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)and (gate adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 10:41
-	1	(gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and (gate adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 11:38
-	1	6596599.pn. and ((anti-reflective adj coating) or (ARC))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 12:08
-	3	(gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and gate and (gate adj dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 12:27
-	1	6117719.pn. and ((anti-reflective adj coating) or (ARC))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 12:10
-	1	6207482.pn. and ((anti-reflective adj coating) or (ARC))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 12:10
-	2	438/595,696,230,778-785.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and gate and (gate adj dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 10:38
-	1	438/366,367,368,369.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and gate and (gate adj dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:14
-	1	438/366,367,368,369,303.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and gate and (gate adj dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 10:37

-	2	5902125.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:40
-	2	5960270.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:43
-	2	5972762.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:44
-	0	6066567pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:44
-	2	6066567.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:45
-	2	6087271.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:50
-	2	6156126.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:50
-	2	6245682.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:51
-	2	6368947.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 14:51
-	0	(gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (dielectric adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and (gate adj stack) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:49
-	2	(anti-reflective adj coating or ARC) and (gate adj stack) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 15:23
-	2	6753242.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/01 15:23
-	2	6066567.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 15:34
-	2	5902125.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 15:36
-	3	597262.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 15:37
-	2	6087271.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 15:55
-	2	6555397.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 15:57

-	1	20000816.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 16:00
-	0	20000814.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 16:35
-	2	6136636.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:34
-	2	61177743.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 16:57
-	2	6372589.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:24
-	2	6368947.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:25
-	2	6245682.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:25
-	2	6156126.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:26
-	2	6097271.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:27
-	2	6087271.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:27
-	2	6066567.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:28
-	2	5972762.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:28
-	2	5960270.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:30
-	2	5902125.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:31
-	2	438/595,696,230,778-785.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:34
-	1	438/366,367,368,369.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC) and gate	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/02 17:34

-	0	6136636.pn. and non-volatile	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:36
-	0	6136636.pn. and memory	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:38
-	0	6136636.pn. and floating	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:38
-	0	@ad<20020319 and (anti-reflective adj coating or ARC) and (gate adj stack) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:50
-	0	@ad<20020319 and (anti-reflective adj coating or ARC) and ((gate adj stack) or (transistor)) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:53
-	0	@ad<20020319 and ((anti-reflective adj coating) or (ARC or BARC)) and ((gate adj stack) or (transistor)) and (non-volatile adj memory adj stack)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:55
-	350	@ad<20020319 and ((anti-reflective adj coating) or (ARC or BARC)) and ((gate adj stack) or (transistor)) and (non-volatile adj memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 09:56
-	48	@ad<20020319 and ((anti-reflective adj coating) or (ARC)) and ((gate adj stack) or (gate adj transistor)) and (non-volatile adj memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 10:02
-	13	@ad<20020319 and ((anti-reflective adj coating) or (ARC)) and ((gate adj stack) or (gate adj transistor)) and (non-volatile adj memory) and spacers	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/03 10:02
-	1	438/366,367,368,369,303.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/06 17:24
-	2	438/595,696,230,778-785.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region) and @ad<20020319 and (anti-reflective adj coating or ARC)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/06 17:24
-	19	438/366,367,368,369,303.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/07 09:10
-	22	438/595,696,230,778-785.ccls. and (gate adj electrode) and (semiconductor adj substrate) and dielectric and source and drain and (oxide adj spacers) and (channel adj region)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/06 17:24